TITLE:

INVESTIGATION OF INTELLIGENCE PARTITIONING IN WIRELESS VISUAL SENSOR NETWORKS

ABSTRACT:

In this thesis, I have explored different possibilities of partitioning the vision processing tasks between hardware, software and locality for the implementation of the visual sensor node, used in wireless visual sensor networks. I have also explored the effect of packets relaying and node density on the energy consumption and implementation of the individual wireless visual sensor node, when used in a multihop wireless visual sensor networks. Wireless visual sensor network is an emerging field which is formed by deploying many visual sensor nodes in the field, where each visual sensor nodes contains image sensor, on board processor, storage capacity and wireless communication link. Compared to the traditional wireless sensor networks which operate on one dimensional data, wireless visual sensor networks operate on two dimensional data which requires higher processing power and communication bandwidth. Unfortunately, the research focus within the field of wireless visual sensor networks have been on two different extremes, involving either sending raw data to the central base station without local processing or conducting all processing locally at the visual sensor node and transmitting only the final results. This research work focuses on determining an optimal point of hardware/software partitioning at the visual sensor node as well as partitioning tasks between local and central processing, based on minimum energy consumption for vision processing tasks. The lifetime of the visual sensor node is predicted by evaluating the energy requirement of the embedded platform with a combination of FPGA and microcontroller for the implementation of the visual sensor node and also taking into account the amount of energy required for receiving/forwarding the packets of other nodes.

Advancements in Field Programmable Gate Arrays (FPGAs) have been the motivation for choosing them as the vision processing platform for implementing visual sensor node. This choice is made due to reduced time-to-market, low non-recurring engineering cost and programmability as compared to ASICs. The other part of the architecture of the visual sensor node is the SENTIO32 platform, which is used both for the software implementation of the visual sensor node and for communicating the results to the central base station using the RF transceiver embedded in it, for the hardware implementation.