ABSTRACT

All who is involved in electronic design knows that one of the critical issues in today's electronic is the power consumption. Designers are always looking for new approaches in order to reduce currents while still retain performance. Floating-gate (FGMOS) circuits have previously been shown to be a promising technique to improve speed and still keep the power consumption low when power supply is reduced below subthreshold voltage for the transistors.

In this thesis, the goal is to determine how good floating-gate circuits can be compared to conventional static CMOS when the circuits are working in subthreshold. The most interesting performance parameters are speed and power consumption and specifically the Energy-Delay Product (EDP) that is a combination of those two. To get a view over how the performance varies and how good the FGMOS circuits are at their best case, the circuits have been designed and simulated for best case performance.

The investigation also includes trade-offs with speed and power consumption for better performance, how to select floating-gate capacitances, how a large circuit fan-in will affect performance and also the influence of different kinds of refresh circuits.

The first simulations of the FGMOS circuits in a 0.13 μm process have several interesting results. First of all, in the best case it is shown that FGMOS has potential to achieve up to 260 times in better EDP-performance compared to CMOS at 150 mV power supply. Continuing with simulations of FGMOS capacitances shows that minimum floating-gate capacitance can be as small as 400 fF and more realistic performance shows that EDP is 37 times better for FGMOS (with parasitic capacitances included). Other aspects of FGMOS design have been to look at how refresh circuits will affect performance (semi-floating-gate circuits) and how a larger fan-in will change noise margin and EDP. It turns out that refresh circuits with the same transistor size does not give a noticeable change in performance while an increase of 8 times in size will give between 5 and 10 times wors EDP. When it comes to fan-in the simulations shows that a maximum fan-in of 5 is possible at 250 mV supply and it decrease to 3 when supply voltage is reduced to 150 mV.

Finally, it should be kept in mind that tuning the performance of FGMOS circuits with trade-offs and by changing the floating-gate voltages to achieve results like the ones stated above will also always affect the noise margins, NM, of the circuits. As a consequence of this, the NM will sometimes be so close to 1 that a fabricated circuit with that NM may not be as functional as simulations suggests. The probability to design functional FGMOS circuits in subthreshold does not seem to be a problem though.