

PhD. Cao Cao licentiate – May 30, 2005

# "Automatic Synthesis of Partitioned FSMs Based on Mixed Synchronous/Asynchronous State Memory"

Main supervisor: Doc Bengt Oelmann - Mittuniversitetet.

Opponent: Prof Per Larsson-Edefors - Chalmers Technical University.

## ABSTRACT

The rapid development of digital circuits with high density and frequency motivates power, in addition to area and speed, to become an important parameter in design constraints. Nowadays, the electronics design industry is confronted by increasingly costly package and cooling systems due to power dissipation. Battery-powered portable devices, such as laptops, mobile phones etc., which provide higher computational capacity and support multi-media information transformation, make the original slim power budget a heavier burden. As synchronous digital design has, over the past few decades, become the industry standard, this new challenge means that asynchronous design techniques must now be reconsidered, as they possess the potential for a reduction in power dissipation.

Finite state machine (FSM) partitioning proves effective for power optimization. In this thesis, a mixed synchronous/asynchronous state memory structure in the decomposed FSM is proposed, which results in implementations with low power dissipation and low area overhead. The state memory is composed of the synchronous local state memory and asynchronous global state memory, where the former is used to distinguish the states inside a sub-FSM, and the latter is responsible for controlling sub-FSM communication. Although asynchronous communication mechanism is introduced between sub-FSMs, the input/output behaviour of the decomposed FSM is still, cycle by cycle, equal to a complete synchronous one. Power consumption can be further reduced by using a clock gating technique and low power state assignment.

Based on this mixed synchronous/asynchronous structure an automatic synthesis tool was developed, which accepts state transition graph (STG) as input and synthesizable VHDL code as output that can be directly used for logic synthesis. An FSM partitioning algorithm, power estimation functions and state encoding optimization aimed at this specific structure are also integrated into the tool to find a low power partitioned FSM within a reasonable run time. The effectiveness of the whole procedure was verified through optimization of standard benchmarks where a power reduction of up to 70% has been demonstrated.